# Behzad Jannati

**M.Sc. Student in Computer Architecture — AI & Hardware Security Researcher**


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## Summary


Driven M.Sc. student in Computer Architecture at the University of Tehran, specializing in the efficient deployment of advanced Artificial Intelligence models on resource-constrained systems. Strong research focus on compressing Vision-Language Models (VLMs) for edge deployment and applying Large Language Models (LLMs) to hardware functional verification and security. Experienced in bridging the gap between deep learning algorithms and hardware platforms (Raspberry Pi, FPGAs).


## Education

**University of Tehran**, Tehran, Iran — Sep 2024 – Sep 2026
*Master of Science in Computer Architecture* — **GPA: 4.0/4.0 (19.5/20)**

- **Thesis:** Compressing VLMs via Layer Analysis and Pruning for Multi-Modal Reasoning on Edge
- **Supervisor:** Prof. Mehdi Kargahi

**Payame Noor University**, Iran — Sep 2018 – Jun 2023
*Bachelor of Science in Computer Engineering* — **GPA: 3.69/4.0 (17.65/20)**

## Research & Academic Experience

**Researcher (Research Assistant)** — Dec 2024 – Present
*Cyber-Physical Systems (CPS/DRTS) Lab, University of Tehran*

- Conducting research on model compression techniques (pruning, quantization, distillation) to deploy large-scale multimodal models on real-world embedded and edge devices.
- Designing hardware-aware AI architectures to optimize performance under resource constraints.

**LLM & Hardware Security Researcher (Academic Project)** — Dec 2024 – Present
*University of Tehran*

- Deployed the **LLaMA 3.1 8B** model using Google Colab and Tesla T4 GPUs to perform inference on complex **Verilog** source codes for automated analysis.
- Investigated hardware security vulnerabilities, focusing on the identification and mitigation of hidden Hardware Trojans using generative AI methodologies.

**Graduate Teaching Assistant** — Oct 2025 – Present
*School of Electrical and Computer Engineering, University of Tehran*

- **Functional Verification of HDL Models (Dr. S. Mohammadi):** Introduced a novel module on LLM applications in verification. Delivered 3 sessions on LLMs, designed bonus assignments on fine-tuning LLMs for assertion generation (VERT dataset), and evaluated constrained-random verification of MIPS processors.
- **Digital Electronics (Dr. Sh. Vahdat):** Designed and conducted hands-on workshops on HSPICE fundamentals, circuit netlists, and gate-level simulations.

## Workshops & Presentations

- **Presenter & Organizer:** *"Functional Verification of HDL Models: An Introduction to Hugging Face LLM Fine-Tuning Using Google Colab"* – University of Tehran (Feb 2026). Bridged traditional hardware verification methodologies with modern AI-driven approaches.

## Honors & Awards

- **Ranked 19th** in the National University Entrance Exam for M.Sc. degree in IT Engineering (Sep 2024).
- **Ranked 129th** in the National University Entrance Exam for M.Sc. degree in Computer Engineering (Sep 2024).

## Technical Skills

- **AI & Machine Learning:** Large Language Models (LLM), Vision-Language Models (VLM), Deep Neural Networks (DNN), RAG, Prompt Engineering, Model Compression.
- **Programming & Hardware:** Python, Verilog, PyTorch, LangChain, HSPICE, Embedded Systems (Raspberry Pi, FPGA).
- **Tools & Frameworks:** Hugging Face, Google Colab, Git/GitHub, LaTeX.

## Certifications

- Retrieval Augmented Generation (RAG) with LangChain – *DataCamp* (Feb 2026)
- Introduction to Python – *DataCamp* (Feb 2026)
- Foundation: Introduction to LangChain (Python) – *LangChain*

## Languages

- **Persian:** Native
- **English:** Professional Working Proficiency (Native/Bilingual equivalent)